AMENDMENTS TO THE CLAIMS:

1. (Cancelled)

2. (Original) A system for estimating the performance of an integrated circuit in a register transfer level, in which the performance of an integrated circuit is estimated based on a net list of a gate level including a signal having correspondence to a logic description of a register transfer level, the system for estimating the performance of an integrated circuit in a register transfer level comprising:

floorplan means for arranging a device model inside of the net list of the gate level within a specified region;

invariable part optimizing means for inserting a buffer based on arrangement information of the floorplan means in order to satisfy a design rule with respect to the signal having the correspondence to the logic description;

interconnection predicting means for predicting the interconnection between devices based on the arrangement information;

performance calculating means for calculating the performance of the net list of the gate level by the use of an interconnection prediction value by the interconnection predicting means; and

display means for displaying the result of the performance calculation, the logic description and the result of a floorplan.

3. (Cancelled)

4. (Original) A system for estimating the performance of an integrated circuit in a register transfer level as claimed in claim 2, further comprising delay recalculating means for

creating the net list whose logic is optimized including the signal having the invariable attribute with respect to a selected path in accordance with a request from the outside, so as to calculate a delay of the path.

5. (Original) A system for estimating the performance of an integrated circuit in a register transfer level, in which the performance of an integrated circuit is estimated based on a net list of a gate level including a signal ~~having correspondence~~ corresponding to a logic description [[of]] in a register transfer level, the system for estimating the performance of an integrated circuit in a register transfer level comprising:

display means for displaying a reach delay time of each of signals, which reaches a partial circuit on [[a]] the net list of a gate level corresponding to a specified portion [[on]] of the logic description.

6. (New) A system for estimating the performance of an integrated circuit in a register transfer level, in which the performance of an integrated circuit is estimated based on a net list of a gate level including information referred by a logic description of a register transfer level, the system for estimating the performance of an integrated circuit in a register transfer level comprising:

display means for displaying a reach delay time of each of signals, which reaches a partial circuit on the net list of a gate level corresponding to a specified portion of the logic description.